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POWER QUALITY IMPROVEMENT IN DISTRIBUTION SYSTEM BY USING DYNAMIC VOLTAGE RESTORER

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Abstract

In this paper, another control methodology in light of current mode control for Dynamic Voltage Restorer (DVR) is proposed to relieve the power quality issues in the supply voltage. The DVR is controlled in a roundabout way by controlling the supply current. The reference supply streams are evaluated utilizing the detected load terminal voltages and the dc transport voltage of DVR. The control conspire depends on synchronous reference outline hypothesis (SRFT) for the operation of a capacitor upheld DVR. The control methodology is confirmed through broad reproduction ponders utilizing MATLAB with its Simulink and Power System Blockset (PSB) tool stash to exhibit the made strides execution of DVR.

Keywords:

Power Quality;
DVR;
Custom Power devices;
Current control.

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1. Introduction

Power quality issues in the dispersion frameworks are tended to in the writing [1-3] because of the expanded utilization of touchy and basic types of gear in the framework. A few illustrations are types of gear of correspondence framework, process businesses, exact assembling forms and so forth. Power quality issues, for example, homeless people, lists, swells also, different mutilations to the sinusoidal waveform of the supply voltage influence the execution of these types of gear. The advancements like custom power gadgets are developed to give assurance against control quality issues. Custom power gadgets are primarily of three classes, for example, arrangement associated compensator like dynamic voltage restorer (DVR), shunt associated compensator, for example, dispersion static compensator (DSTATCOM), and a blend of arrangement and shuntconnected compensators known as brought together power quality conditioner (UPQC) [2, 4-6]. The arrangement associated compensator can manage the heap voltage from the power quality issues, for example, droop, swell and so forth in the supply voltage. Subsequently it can shield the basic shopper loads from stumbling and ensuing loss of generation [2]. The custom power gadgets are

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created and introduced at the purchaser point to meet the power quality models, for example, IEEE-519 [7].

A DVR is utilized to remunerate the supply voltage aggravations, for example, list and swell. The DVR is associated between the supply and delicate burdens, with the goal that it can infuse a voltage of required greatness and recurrence in the dispersion feeder. The DVR is worked to such an extent that the heap voltage size is managed to a consistent greatness, while the normal genuine power ingested/provided by it is zero in the enduring state. The capacitor upheld DVR is generally tended to in the writing [8-13]. The prompt responsive power hypotheses (IRPT) [6], sliding mode controller [9], immediate symmetrical segments [2, 13] and so on, are talked about in the writing for the control of DVR. In this paper another control calculation is proposed in view of the present mode control and relative necessary (PI) controllers for the control of DVR. The broad recreation is performed to show its ability, utilizing the MATLAB with its Simulink and Power System Blockset (PSB) tool compartments.

2. Principle of operation of DVR:

The single line chart of a framework with the DVR associated in arrangement with the supply is appeared in Fig. 1 (a). The DVR infuses a voltage (Vc) in arrangement with the terminal voltage (Vt) with the goal that the heap voltage (VL) is constantly consistent in extent. Fig. 1(b) demonstrates the phasor outline of DVR when the terminal voltage is having hang (Vt) and swell ($Vt^{'}$) in the voltage. The schematic chart of a three stage DVR associated with a three stage 3-wire framework is appeared in Fig. 2 (a). The source impedances (Za, Zb, Zc) are between the source and the terminal. The DVR utilizes three single-stage transformers (Tr) to infuse voltages in arrangement with the terminal voltage.

A voltage source converter (VSC) alongside a dc capacitor (C_{dc}) is utilized to understand a DVR. The inductor in arrangement (L_r) and the parallel capacitor (C_r) with the VSC are utilized for diminishing the swell in the infused voltage. Fig. 2(b) demonstrates the phasor chart for the infused voltage and the principal voltage drop to keep up the dc transport voltage of DVR. VL' and IL' are the heap voltage and current before the droop happened in the supply framework. After the list occasion, the extent of the heap voltage (V_L), the heap current (I_L) and the power factor point (Θ) are unaltered, however a stage hop is happened from the pre-hang condition. The infused voltage (V_c) has two segments. The voltage infused at quadrature (V_{cq}) with the current is to keep up the heap voltage at consistent size and the in-stage voltage (V_{cd}) is to keep up the dc transport of VSC and furthermore to meet the power misfortune in the DVR. The control procedure of the DVR is to accomplish these two segments of the infusion voltage and this is accomplished by controlling the supply current. The streams are detected and the two segments of ebbs and flows, one is the segment to keep up the dc transport voltage of DVR and the second one is to keep up the heap terminal voltages, are included with the detected load current to appraise the reference supply current.

3. DVR control strategy:

The proposed calculation depends on the estimation of reference supply streams. It is like the calculation for the control of a shunt compensator like DSTATCOM for the terminal voltage control of straight and nonlinear burdens [6]. The proposed control calculation for the control of DVR is delineated in Fig. 3. The arrangement compensator known as DVR is utilized to infuse a voltage in arrangement with the terminal voltage. The list and swell in terminal voltages are remunerated by controlling the DVR and the proposed calculation innately gives a self-supporting dc transport for the DVR. Three-stage reference supply streams (isa*, isb*,isc*) are determined utilizing the detected load voltages (v_{la}, v_{lb}, v_{lc}), terminal voltages (vta, vtb, vtc) and dc transport voltage (vdc) of the DVR as input signals.

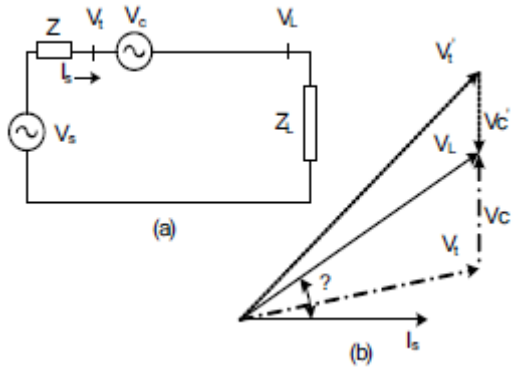

Figure 1 *(a) Single line diagram of DVR (b)Phasor diagram*

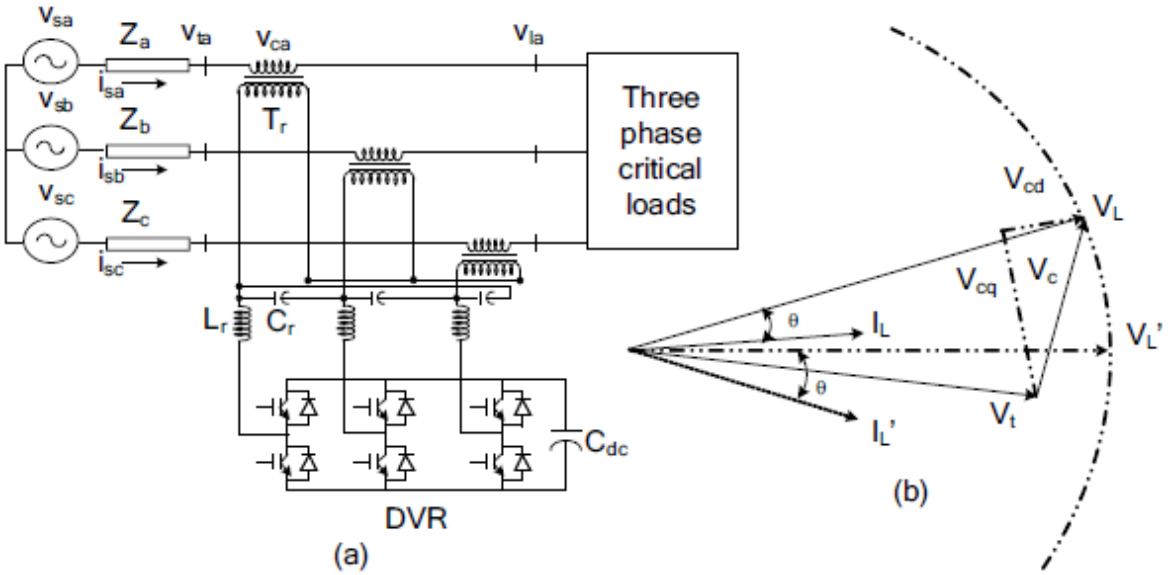

Figure 2 *(a) Three phase DVR scheme (b) Phasor diagram*

The synchronous reference outline hypothesis based technique is utilized to get the immediate pivot (id) and quadrature hub (iq) segments of the heap current. The heap streams in the three-stages are changed over into the d-q-0 outline utilizing the Park's change as,

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & -\sin\theta & \frac{1}{2} \\ \cos\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta-\frac{2\pi}{3}\right) & \frac{1}{2} \\ \cos\left(\theta+\frac{2\pi}{3}\right) & \sin\left(\theta+\frac{2\pi}{3}\right) & \frac{1}{2} \end{bmatrix}\begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix}$$

A three-stage PLL (stage bolted circle) is utilized to synchronize these signs with the terminal voltages (vta, vtb, vtc). The d-q segments are then gone through low pass channels to extricate the dc segments of id and iq. The blunder between the reference dc capacitor voltage and the detected dc transport voltage of DVR is given to a PI (relative basic) controller of which yield is considered as the misfortune segment of current and is added to the dc part of id. Thus, a moment PI controller is utilized to direct the plentifulness of the heap voltage (Vt). The adequacy of the heap terminal voltage is utilized over the reference sufficiency and the yield of PI controller included with the dc part of iq. The resultant streams are again changed over into the reference supply ebbs and flows utilizing the turn around Park's change. Reference supply streams (isa*, isb*,isc*) and the detected supply ebbs and flows (isa, isb, isc) are utilized as a part of PWM current controller to produce gating beats for the switches. The PWM controller works at a recurrence of 10kHz and the gating signals are given to the three-leg VSC for the control of supply streams.

4. Modelling and Simulation:

The DVR is demonstrated and mimicked utilizing the MATLAB and its Simulink and Power System Blockset (PSB) tool compartments. The MATLAB model of the DVR associated framework is appeared in Fig. 4. The three-stage source is associated with the three-stage stack through arrangement impedance and the DVR. The considered load is a slacking power factor stack. The VSC of the DVR is associated with the framework utilizing an infusion transformer. What's more, a swell channel for separating the exchanging swell in the terminal voltage is associated over the terminals of the auxiliary of the transformer. The dc transport capacitor of DVR is chosen in view of the transient vitality prerequisite and the dc transport voltage is chosen in light of the infusion voltage level. The dc capacitor chooses the swell substance in the dc voltage. The framework information is given in Appendix.

The proposed control calculation is demonstrated in MATLAB as appeared in the figure 5. The reference supply streams are gotten from the detected load voltages, supply ebbs and flows and dc transport voltage of DVR. The yield of the PI controller utilized for the control of dc transport voltage of DVR is included with the immediate pivot segment of current. Correspondingly, the yield of the PI controller utilized for the control of the sufficiency of the heap voltage is included with the quadrature pivot segment of the supply current. A heartbeat width adjustment (PWM) controller is utilized over the mistake between reference supply streams and detected supply ebbs and flows to create gating signals for the IGBT's (protected entryway bipolar transistors) of the VSC of DVR.

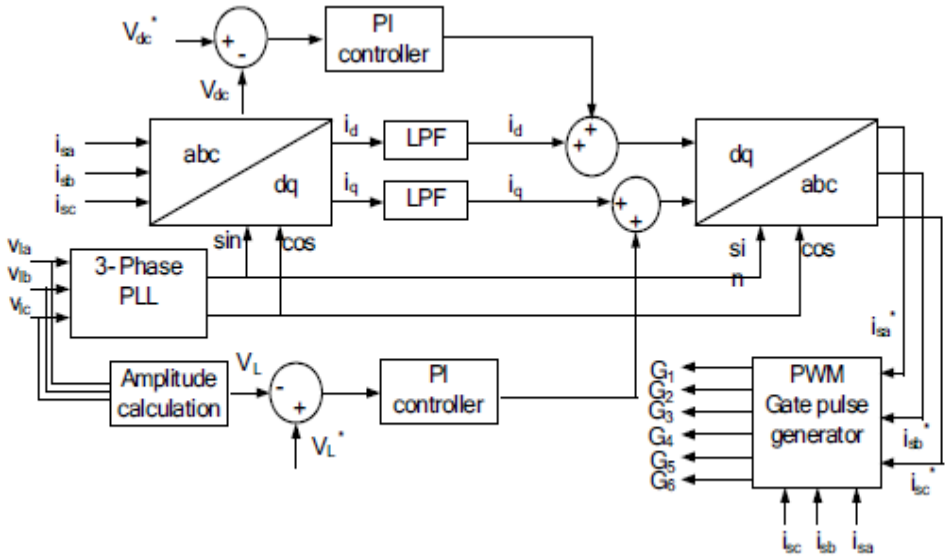

Figure 3 Control scheme of DVR

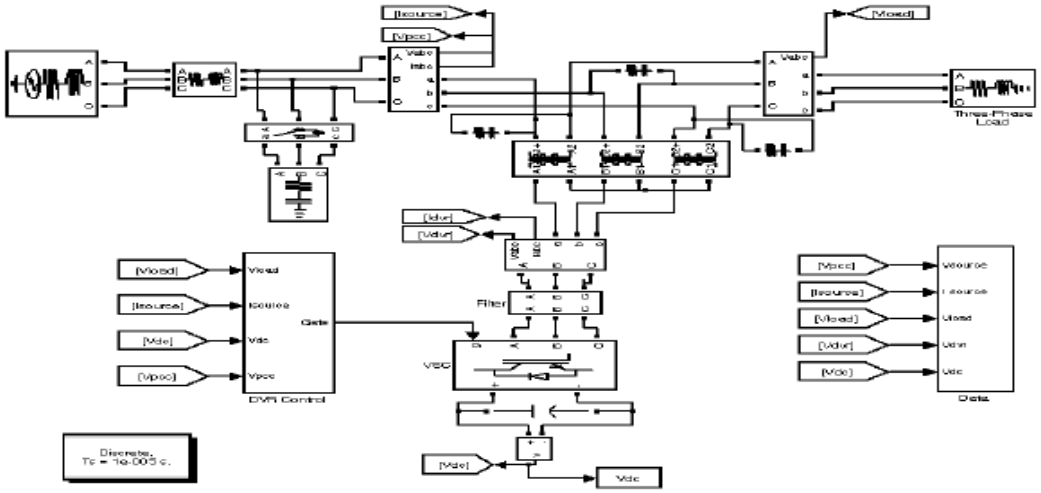

Figure 4MATLAB Based model of the three phases DVR connected system

5. Results and Discussions:

The proposed control plan of DVR is confirmed through recreation utilizing MATLAB programming alongside its Simulink and Power System Blockset (PSB) tool stash. The DVR is tried under various working conditions like droop (Fig. 6) and swell (Fig. 7) at the terminal voltages (vta, vtb, vtc). In Fig. 6, the terminal voltage has a hang of 30% with a greatness at 70% of appraised an incentive at 0.26 sec and happens up to 0.45 sec. The DVR infuses principal voltage (vc) in arrangement with the terminal voltages (vla, vlb, vlc). The heap voltage is kept up at the evaluated esteem. The terminal voltage (vt), supply current (is), abundancy of terminal voltage (Vt) the adequacy of load voltage (VL) and the dc transport voltage (vdc) of DVR are likewise appeared in the Fig. 6. It is watched that the dc transport voltage of DVR is kept up at reference esteem.

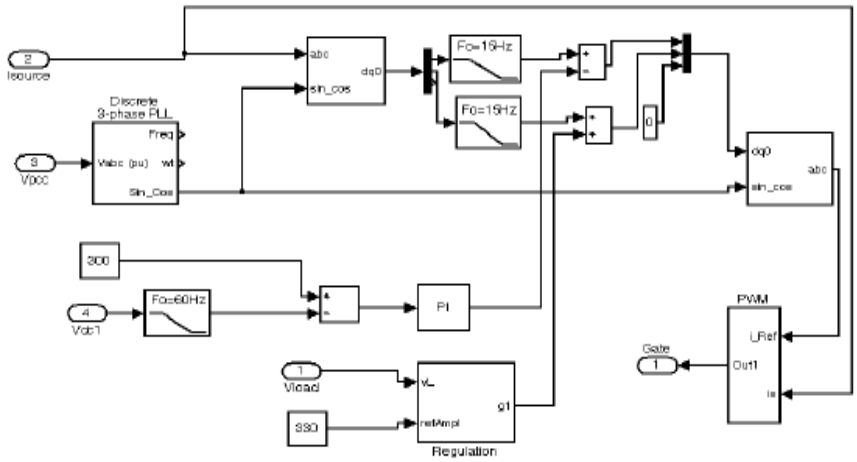

Figure 5 MATLAB Based model of the proposed control method

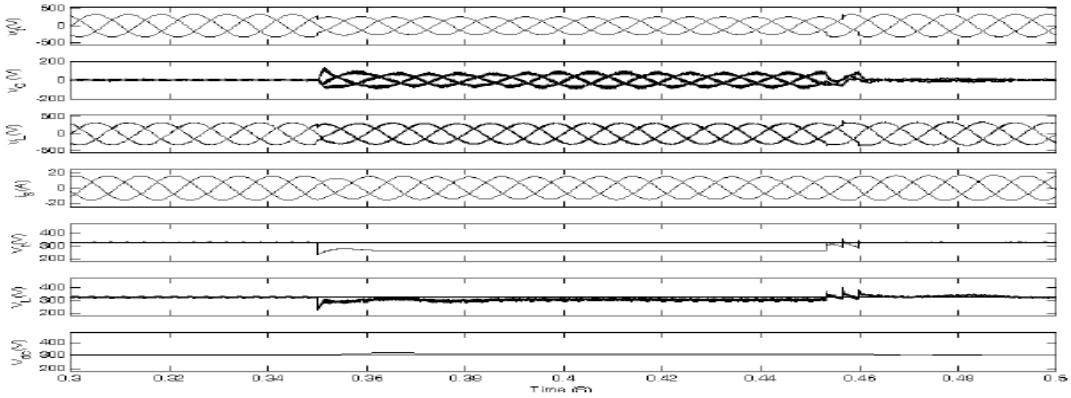

Figure 6 Dynamic behaviour of DVR for voltage sag compensation

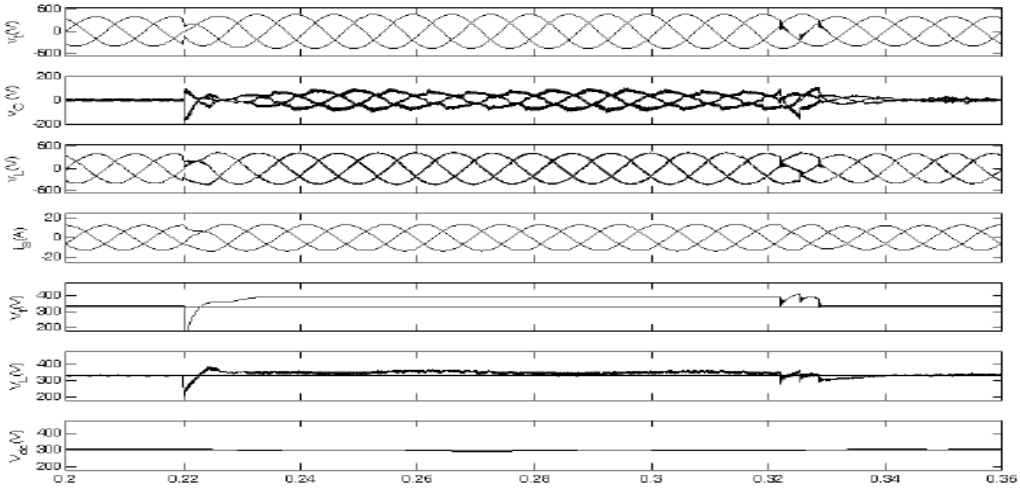

Figure 7 Dynamic behaviour of DVR for voltage swell compensation

Similarly, in fig 7, a swell in terminal voltage (V_t) has occurred at 0.22sec upto 0.32sec and the load voltage (V_l) is observed to be satisfactory due to the proper voltage injection by the DVR. The heap voltage (vL) is kept up at the appraised esteem. The terminal voltage (vt) supply current (is), the plentifulness of terminal voltage (Vt), the abundancy of the heap voltage (VL) and the dc transport voltage (vdc) of DVR are likewise appeared in the Fig. 7. It is watched that the dc transport voltage of DVR is kept up at reference esteem; however bother is happening amid drifters.

6. Conclusions:

Another control procedure in light of current mode control for Dynamic Voltage Restorer (DVR) has been proposed to alleviate the power quality issues in the terminal voltages. The proposed control plan of DVR has been approved the remuneration of hang and swell in terminal voltages. The execution of the DVR has been found good to alleviate the voltage control quality issues. Additionally, it has been discovered competent to give self bolstered dc transport of the DVR through power exchange from air conditioning line at key recurrence.

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